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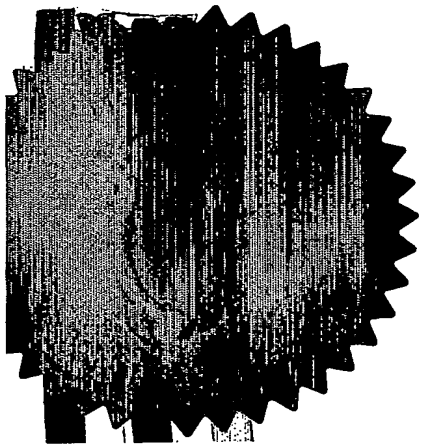
Application No.	S2002/0221
Date of Filing	27th March 2002
Applicant	Commergy Technologies Limited, an Irish Company of 133 Lansdowne Park, Ballsbridge, Dublin 4, Ireland

Dated this 14TH day of April 2003.

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)



Brenan McKeevney

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APPLICATION No. 5020221

FORM NO. 1

REQUEST FOR THE GRANT OF A PATENT

PATENTS ACT 1992

The Applicant(s) named herein hereby request(s)
[ ] the grant of a patent under Part II of the Act
[X] the grant of a short-term patent under Part III of the Act
on the basis of the information furnished hereunder.

1. Applicant(s)

COMMERGY TECHNOLOGIES LIMITED
133 Lansdowne Park
Ballsbridge
Dublin 4
Ireland.
an Irish company

2. Title of Invention
A power converter design

3. Declaration of Priority on basis of previously filed application(s) for same invention (Sections 25 & 26)

Previous Filing Date	Country in or for which filed	Filing No.

4. Identification of Inventor(s)

Name(s) and addresse(s) of person(s) believed by the Applicant(s) to be the inventor(s)
George Young,
an Irish Citizen of 11 Woodlands Park, Blackrock, County Dublin, Ireland.

5. Statement of right to be granted a patent (Section 17(2) (b))

The Applicant derives the right to apply by virtue of a Deed of Assignment dated March 26, 2002

6. Items accompanying this Request

(i)	[X]	prescribed filing fee (Euro 60.00)
(ii)	[ ]	specification containing a description and claims
	[X]	specification containing a description only
	[X]	Drawings referred to in description or claims
(iii)	[ ]	An abstract
(iv)	[ ]	Copy of previous application(s) whose priority is claimed
(v)	[ ]	Translation of previous application whose priority is claimed
(vi)	[X]	Authorisation of Agent (this may be given at 8 below if this Request is signed by the Applicant(s))

7. Divisional Application(s)
The following information is applicable to the present application which is made under Section 24 -

Earlier Application No.
Filing Date:

8. Agent

The following is authorised to act as agent in all proceedings connected with the obtaining of a patent to which this request relates and in relation to any patent granted -

Name & Address

Cruickshank & Co. at their address recorded for the time being in the Register of Patent Agents is hereby appointed Agents and address for service, presently 1 Holles Street, Dublin 2.

9. Address for service (if different from that at 8)

Signed Cruickshank & Co.

By:- Michael Lucas Executive.

Agents for the Applicant

Date March 27, 2002.

"A Power Converter Design"

Introduction.

The present invention relates to a power converter comprising input supply voltage connected to a rectifier having a number of field effect transistor (FET) switches and a filter and an output rectified supply voltage. The invention is in particular directed towards providing a power converter to eliminate switch-on and switch-off losses and common mode noise associated with power converters.

Power converters are required to convert voltages to different levels within electronic systems. The problem with power converters is that when a power converter is turned on it normally involves the simultaneous turn off a diode element subject to reverse recovery flow. A problem with the design of these converters is that the rate of current rise needs to be controlled. Another problem with converters is that on turn-off a switch, typically a field effect transistor (FET), the gate of the FET is typically brought to zero volts but the leakage inductance causes the source of the FET to go negative until the energy in this leakage is discharges, which means current flows for an extended period. Depending on the power converter parameters the voltage rise may overlap with a slow decaying current "tail", which can result in severe turn-off loss in the converter.

A widely used power converter is a DC-DC converter. Common mode noise is a problem associated with DC-DC converters. In a typical power converter common mode noise is reduced by keeping all voltages appearing across transformer capacitance's "balanced", so that the output ground is kept as close to the potential of the input ground connection. This is usually facilitated by the use of "double-ended" configurations where voltage excursions by one part of the winding are often balanced by excursions of another part of the winding. This is achieved quite readily in topologies such as the push-pull where there is excellent cancellation due to the semetry of the input winding. However, in some configurations the whole output winding "moves" relative to output ground thus giving a clear common mode voltage differential and associated current flows, which leads to common mode noise within

the power converter.

The object of the present invention is therefore to provide a power converter design to eliminate losses associated with the turn-on and turn-off of switches within a converter while also eliminating common mode noise associated with power converters.

Statements of Invention.

According to the present invention there is provided a power converter comprising an input supply voltage connected to a rectifier having a number of field effects transistor (FET) switches and a filter and an output rectified supply voltage characterised in that there is provided a current transformer positioned near the source one of the switching FETs to provide a leakage inductance to control the rate of current rise on switch-on of the switching FET.

The advantage of the current transformer is that it provides a leakage inductance so that the current rise is controlled and eliminates reverse recovery flows that are present in turning on a power converter.

In another embodiment of the present invention a diode is connected to the primary side of the current transformer. The advantage of having a diode is that it provides a discharge path for energy stored in the leakage inductance on switch off of the FET switch.

In another embodiment of the present invention there is provided a power converter comprising an input supply voltage connected to a rectifier having a number of FET switches and a filter and an output rectified supply voltage characterised in that there is provided a capacitor connected between the input ground and output ground of the power converter to attenuate a common mode signal to reduce common mode noise effects in the power converter.

Preferably there is connected to the capacitor is an auxiliary winding

In a further embodiment a neutralising signal is associated with the capacitor to cancel any interference signals in the power converter.

Detailed Description of the Invention.

The invention will be more clearly understood from the following description of some embodiments thereof, given by way of example only, with reference to the accompanying drawings, in which: -

Fig. 1 is a block diagram of the power converter design of the present invention.

Fig. 2 shows one embodiment of the present invention with a current transformer with an associated diode connected to one of the switches of the power converter.

Fig. 3 illustrates another embodiment of the present invention to reduce the common mode noise in the power converter.

Fig. 4 is a graph of the voltage between the centre point of the output winding and ground of the power converter.

Referring now to Fig. 1 there is illustrated a block diagram of the power converter design illustrated generally by the reference 1. The power converter 1 has an independent bias supply for drive circuitry and uses a main controller located on the secondary side feeding the drive signal back to the main switches in the primary side. Referring now to Fig. 2 there is illustrated part of the power converter design generally indicated by the reference 10. A current transformer 11 has its primary connected to the source of one of the switches 13 of the power converter. The switch can be a field effect transistor (FET) or a MOSFET switch, all of which are readily known in the field of power converters. A diode 12 is connected in parallel with the primary of the current transformer 11.

When turning on a power converter, particularly one which involves the simultaneous turn-off of a diode element subject to reverse recovery current flows the rate of current rise needs to be controlled.

The present invention carries out this quite readily through utilising the leakage inductance of the current transformer 11 connected to the source of the switching FET switch 13.

In operation, the on-switching action of the FET switch 13 in the presence of the leakage inductance is as follows. The gate driver pulls up the gate through a gate drive resistor. The source also rises as a voltage is developed across the source-lead leakage inductance. The voltage across gate-source is maintained approximately at the threshold level. This gives a voltage – for example 3V to 4V, across the leakage inductance. With a leakage inductance of 30nH and this applied voltage, the rate of change of current is given by V=L (di/dt) or (di/dt) is 1.67×10^8 A/s. With a turns-ratio of 4:1 this corresponds to a secondary-side rate of change of 660A/us, which is a figure for which reverse recovery performance is specified. The rate of current change is of course also influenced by the choice of gate drive resistor. The slow current rise occurs as the voltage drops resulting in reducing in reduced turn-on loss.

The energy represented by the leakage inductance must also be dissipated on turn-off. With 30nH leakage inductance and 10A turn-off current at 200KHz, the energy lost is given by $0.5LI^2$, or 300mW.

The present invention addresses this issue by placing the diode 12 across the current transformer 11 winding. The diode 13 does not affect the beneficial current-rise slowing action on turn-on, allowing the source to rise. It prevents the source form going below ground on turn-off and provides a discharge path for energy stored in the leakage inductance.

Referring now to Figs. 3 and 4 and initially to Fig. 2, there is illustrated a power converter design of the present invention indicated generally by the reference 20, in which there is provided an additional capacitor 21 connected between an input ground

22 and the output ground 23 of the power converter 20.

The winding arrangement as illustrated in Fig. 3, where a waveform opposite to that shown in Fig. 4 but double the amplitude is created. This may then be coupled to the input ground by the capacitor 21, which is half the value of the capacitance between input and output windings of the transformer 24 in order to cancel common mode currents. The capacitor 21 may be implemented as a discrete component or integrated within a printed circuit board. In a planar magnetic implementation the "winding" consists of simple tracking.

The common mode signal may be attenuated using a capacitive potential divider by fitting capacitors between the input ground 22 and output ground 23. An effective compliment to this approach involves injecting a neutralising signal with the capacitor 21 to cancel any interfering signal.

It will be appreciated in the case of the twin inductor output rectifier configuration commonly known as a current doubler, which is illustrated on Fig. 3, the output winding is alternatively completely at output ground or one end is lifted to the level of the transformer 24 output stage. The next effect is to have the complete winding moving between 0 and half the transformer output level. For example, in the case of a 48 Volt input converter with a 4:1 turns ratio the voltage and the winding varies between 0 and 6 volts. It will be appreciated given the large capacitance value that maybe employed in modern converters using planar magnetics, this voltage level imposes design criteria in the amount of external filtering required to achieve EN 55022 and other similar standards.

In the specification the terms "comprise, comprises, comprised and comprising" or any variation thereof and the terms "include, includes, included and including" or any variation thereof are considered to be totally interchangeable and they should all be afforded the widest possible interpretation. The term theoretical refers to the scientific community and not the inventor.

The invention is not limited to the embodiments hereinbefore described but may be varied in both construction and detail.

PS205.Mar.15

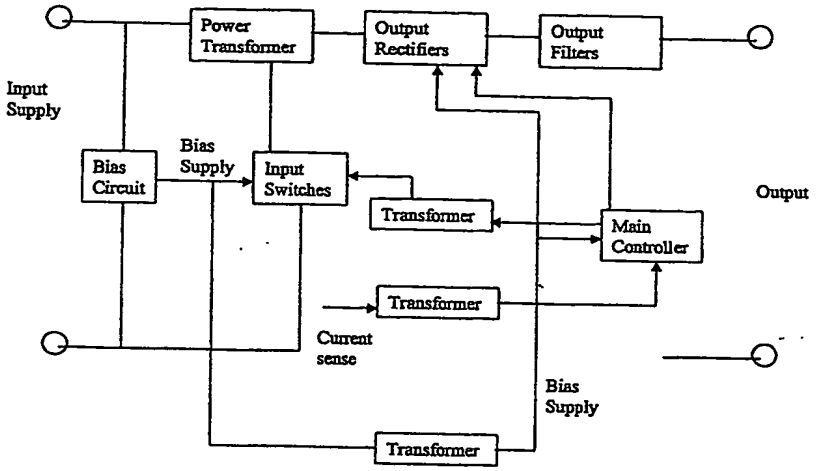
Power Transformer
Output Rectifiers
Output Filters
Input Supply
Bias Circuit
Bias Supply
Input Switches
Transformer
Main Controller
Output
Transformer
Current sense
Bias Supply
Transformer
1

Fig 1

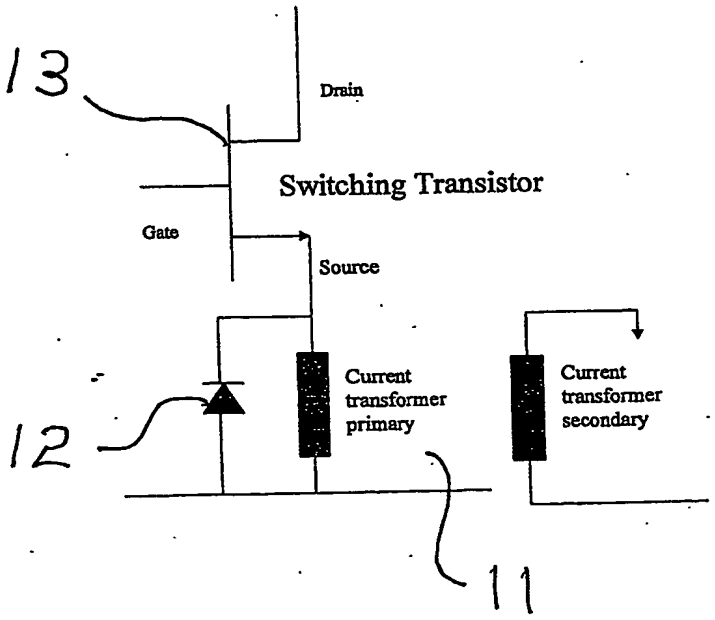
13
Drain
10
Switching Transistor
Gate
Source
Current transformer primary
Current transformer secondary
12
11

Fig 2

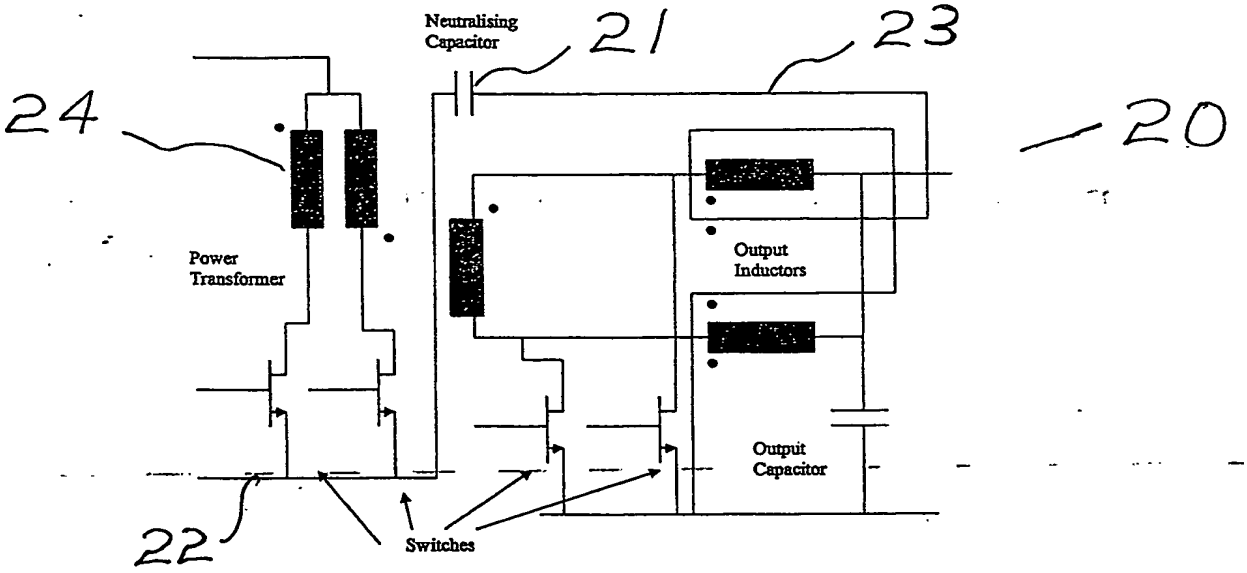
Neutralising
Capacitor
21
23
24
20
Power
Transformer
Output
Inductors
Output
Capacitor
22
Switches

FIG 3

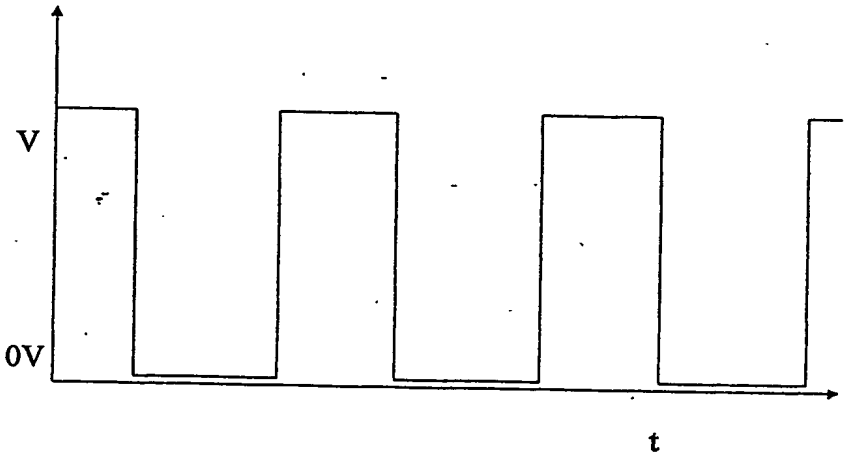
V
0V
t

FIG 4